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I Claim:

1. A synchronization device for a semiconductor memory device, comprising:

a temperature-controllable delay device for assisting in time modulating an input clock signal, said temperature-controllable delay device one of receiving and generating the input clock signal, said temperature-controllable delay device further generating a signal delay dependent on an operating temperature of the semiconductor memory device, said temperature-controllable delay device outputting an output clock signal based on the input clock signal with a delay equal to the signal delay.

2. The synchronization device according to claim 1, wherein the signal delay can be generated satisfying a relationship:

$$Cout(t) = Cin(t-\Delta t(\theta))$$

for the input clock signal and the output clock signal, where Cin is the input clock signal, Cout is the output clock signal being a time-dependent output clock signal, t is time, Δt is the signal delay, and θ is the operating temperature.

3. The synchronization device according to claim 1, wherein the signal delay dependent on the operating temperature is

generated such that the output clock signal or a time characteristic of the output clock signal is substantially independent of the operating temperature of the semiconductor memory device.

4. The synchronization device according to claim 1, wherein said temperature-controllable delay device generates a first signal delay $\Delta t(\theta 1)$ and a second signal delay $\Delta t(\theta 2)$ for each first operating temperature $\theta 1$ and for each second operating temperature $\theta 2$ of the semiconductor memory device, respectively, such that a relationship

$$Cout1(t) = Cout2(t)$$

is satisfied by output clock signals Cout1 and Cout2 for all times t, provided that

$$Cin1(t) = Cin2(t)$$

is satisfied by respective input clock signals Cin1 and Cin2 for all the times t.

5. The synchronization device according to claim 1, wherein said temperature-controllable delay device generates a relatively shorter signal delay given a relatively higher operating temperature of the semiconductor memory device, and

generates a relatively longer signal delay given a relatively lower operating temperature of the semiconductor memory device.

- 6. The synchronization device according to claim 1, wherein said temperature-controllable delay device uses a temperature signal representing the operating temperature of the semiconductor memory device for a temperature-dependent controlling of the signal delay.
- 7. The synchronization device according to claim 6, further comprising a control line over which the temperature signal is supplied.
- 8. The synchronization device according to claim 7, further comprising a temperature sensor generating the temperature signal and connected to said control line.
- 9. The synchronization device according to claim 1, further comprising a delay line with an input terminal, an output terminal, and a control terminal, said temperature-controllable delay device has an input terminal and an output terminal disposed in said output terminal of said delay line.
- 10. The synchronization device according to claim 9, further comprising:

a feedback device connected to said temperature-controllable delay device and having an input terminal and an output terminal; and

a phase detector connected to said feedback device and having first and second input terminals and an output terminal.

- 11. The synchronization device according to claim 10, wherein said input terminal of said feedback device is connected to said output terminal of said temperature-controllable delay device in said output terminal of said delay line, said output terminal of said feedback device is connected to said first input terminal of said phase detector.
- 12. The synchronization device according to claim 10, wherein:

said second input terminal of said phase detector is connected to said input terminal of said delay line; and

said output terminal of said phase detector is connected to said control terminal of said delay line.

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13. The synchronization device according to claim 1, wherein said temperature-controllable delay device has two tri-state inverters that are connected in series.

- 14. The synchronization device according to claim 6, wherein the temperature signal is a control voltage.
- 15. The synchronization device according to claim 1, wherein the semiconductor memory device is selected from the group consisting of a high-frequency semiconductor memory device and a DDR-RAM memory module.
- 16. A semiconductor memory device, comprising:
- a synchronization device for time-modulating a clock signal, said synchronization device including:
 - a temperature-controllable delay device for assisting in time modulating an input clock signal, said temperature-controllable delay device one of receiving and generating the input clock signal, said temperature-controllable delay device further generating a signal delay dependent on an operating temperature of the semiconductor memory device, said temperature-controllable delay device outputting an output clock signal based on the input clock signal with a delay equal to the signal delay.